YOR920030328US1 YOR.484

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Guy Moshe Cohen

Serial No.: 10/645,646 Group Art Unit: Not Yet Assigned

Filing Date: August 22, 2003 Examiner: Unknown

For: STRAINED-CHANNEL FIN FIELD EFFECT TRANSISTOR (FET) WITH A UNIFORM CHANNEL THICKNESS AND SEPARATE GATES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Assignee's Deposit Account No. 50-0510.

Respectfully submitted,

Sean M. McGinn
Registration No. 34,386

Date: 11/10/03

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
YOR920030328US1	10/645,646
Applicant(s)	
Guy Moshe Cohen	
Filing Date	**Group Art Unit**
August 22, 2003	Not Yet Assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,413,802 B1	07/02/02	Hu et al.			
		6,593,625 B2	07/15/03	Christiansen et al.			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Yang-Kyu Choi, Tsu-Jae King, Chenming Hu, "Spacer FinFET: nanoscale double-gate CMOS technology for the terabit era", Solid-State Electronics, 46, pp. 1595-1601, 2002.
		K. Rim, J.L. Hoyt, J.F. Gibbons, "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's", IEEE Trans. Electron Devices, 47(7), p. 1406-1415.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		P.M. Mooney, "Strain Relaxation and Dislocations in SiGe/Si Structures", Materials Science & Engineering, R Reports: A Review Journal, Continuation of Materials Science Reports, Volume R17, No. 3, pp. 105-146, (1996).

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